Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-7 (Canceled)

8. (Original) An integrated circuit on a crystalline silicon substrate of a first conductivity type for operating over a temperature range of T_1 to T_2, including an ion implanted resistor formed in the crystalline silicon substrate of the opposite conductivity type, the resistor being isolated from the rest of the substrate by a PN junction and having an implantation dose providing a minimum resistance at a temperature of approximately $(T_1 + T_2)/2$.

9. (Original) The integrated circuit of claim 8 wherein the silicon substrate is a p-type substrate and the resistor body is formed by arsenic implantation.

10. (Original) The integrated circuit of claim 9 wherein the temperature T_1 is –40C and T_2 is +85C.

11. (Original) The integrated circuit of claim 8 further comprising first and second heavily doped regions of the same conductivity type as the resistor body providing first and second contacts to the resistor.

12. (Original) The integrated circuit of claim 11 further comprising an insulating layer over the resistor with contact openings therein to provide access to the first and second heavily doped regions, and a patterned metal layer there over providing electrical contact to the heavily doped regions.

13. (Original) The integrated circuit of claim 8 wherein the integrated circuit is a CMOS integrated circuit.

14. (Original) The integrated circuit of claim 8 wherein the integrated circuit comprises a bipolar integrated circuit.

15. (Original) The integrated circuit of claim 8 wherein the minimum resistance is within 20C of the temperature of $(T_1 + T_2)/2$.

16. (Original) The integrated circuit of claim 8 wherein the minimum resistance is within 10C of the temperature of $(T_1 + T_2)/2$.

17. (Original) The integrated circuit of claim 8 wherein the minimum resistance is within 5C of the temperature of $(T_1 + T_2)/2$.

18. (Original) The integrated circuit of claim 8 wherein the resistances of the resistor at the two temperature extremes are within 1% of each other.

19. (Original) The integrated circuit of claim 8 wherein the resistances of the resistor at the two temperature extremes are within 0.5% of each other.

20. (Original) The integrated circuit of claim 8 wherein the resistances of the resistor at the two temperature extremes are within 0.25% of each other.

Claims 21-33 (Canceled)